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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,845	01/23/2001	Kiyotoshi Ueda	50090-265	1553

7590 04/11/2003

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EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,845	UEDA ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *6 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5,7-11,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's request for reconsideration of the restriction requirement of the last Office action is persuasive and, therefore, the restriction requirement of that action is withdrawn.

Claims 1-5, 7-11 and 13-14 will be Examine here.

Claim Objections

Claim 7 is objected to because of the following informalities: "correcting means" should read --calibration means--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5, 7-11 and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, Examiner has following question/concern: it is unclear who/what generates a trigger signal? and who/what reads the stored data?

Regarding claim 3, it is unclear what/how calibration data file is created?

Regarding claim 4, it is not clear what is functional test?

Regarding claim 7, it is not clear what is "input waveform timing"? Who measures the measuring signal and how that device is related to correcting means?

All claims that depend from these rejected claims are also rejected.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-9, 11 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Otsuji et al. (US 4928278).

Regarding claims 1-2 and 7, Otsuji et al. (hereunder Otsuji) in fig. 1-8 discloses: a semiconductor integrated circuit testing apparatus for testing signal wiring length connecting to all pins [lines 4-6 of column 18] of a semiconductor integrated circuit, comprising:

a signal generator [A] configured to generate a measuring signal and to transmit the measuring signal to all pins of the semiconductor integrated circuit [lines 40-54 of column 7]; and

correcting means [3, 4, B, 8 and 2] for correcting input waveform timing based on measurements of the measuring signal.

Regarding claims 5 and 8, Otsuji discloses said correcting means includes:

Clock generating means [2] for generating a clock signal (high speed for claim 5);

latching means [3] for latching said measuring signal by use of said clock signal from said clock generating means;

storing means [6] for storing as data said measuring signal latched by said latching means. and

controlling means [8] for retrieving the data held in said storing means for output to an external entity.

Regarding claim 9, Otsuji discloses: said latching means, said storing means and said controlling means are incorporated in said semiconductor integrated circuit [lines 40-44 of column 7].

Regarding claim 11, Otsuji discloses: said clock generating means is a high-speed clock generating circuit [2 and lines 10-30 of column 19] for generating a high-speed clock signal.

Regarding claims 13-14, Otsuji discloses: the semiconductor integrated circuit fabricated by use of a semiconductor integrated circuit testing apparatus [lines 40-44 of column 7].

Regarding claim 3, Otsuji discloses: the step of creating a calibration data file based on the data sent to said tester [lines 55-68 of column 7]

Regarding claim 4, Otsuji discloses: the step of referencing said calibration data file to correct waveform timing of said measuring signal upon functional test performed by said tester [lines 55-68 of column 7].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuji as applied to claims 8 and 7 above.

Regarding claim 10, Otsuji also discloses: a terminating circuit [inherent to lines 11-31 of column 8 and element 3], latching circuit [inherent to element 3] and storing means [6]. Otsuji do not disclose FIFO memories and scan FF circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use of FIFO memories and scan FF circuits in storing circuit, since it was well known in the art (see US 4688211, Aug. 18, 1987) that memories and scan circuits are used to temporary storing of mismatch or any other data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
April 4, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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